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Description

TEST KET LAYOUT FOR PRECISELY MONITORING 3-FOIL LENS ABERRATION EFFECTS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to monitoring of lens aberration during a semiconductor process, and more particularly, to a test key layout for precisely monitoring a 3-foil lens aberration during the fabrication of deep-trench capacitor memory devices by eliminating the COMA aberration.

[0003] 2. Description of the Prior Art

[0004] The relentless drive in the integrated circuit industry toward greater packing density and higher speeds has served as the impetus for optical lithography to reduce printed image sizes. Deep-UV (DUV) lithography has been developed to scale minimum feature sizes of devices on

semiconductor chips to sub-micron dimensions. However, all optical projection systems for micro-lithography depart from perfection because of various lens aberrations, especially when large image field size is combined with high numerical aperture (NA). Such aberrations have a variety of effects on lithographic imaging: shifts in the image position, image asymmetry, reduction of the process window, and the appearance of undesirable imaging artifacts. These undesirable effects are sometimes exacerbated through use of resolution enhancement techniques such as phase-shift masks or nonstandard illumination. Consequently, the lens aberration monitoring system plays an important role in the semiconductor processes.

[0005] Fig.1 illustrates an enlarged plan view of a prior art test key layout 10 for monitoring lens aberrations that occur during the fabrication of deep trench (DT) capacitor devices. As shown in Fig.1, the test key layout 10 comprises a plurality of DT test pairs including pair A, pair B, and pair C. Each of the pairs A, B, and C comprises a left side DT pattern 12 and a right side DT pattern 14. Typically, both of the left side DT pattern 12 and right side DT pattern 14 are rectangular shaped and, as specifically indicated, have a length L and width W. According to the prior

art, pair A is disposed at a center position of the test key area 20, the pair B is arranged in 45 degree direction with respect to the pair A in the test key area 20, while the pair C is disposed in 45 degree direction with respect to the pair B. The pair A and pair C are aligned with a reference Y-axis. As seen, pair C is disposed a distance from the pair A along the ±Y-axis. In the indicated circle region 30, i.e., the area substantially surrounded by the pair A and pair B, no DT test pair is disposed therein. Typically, the lens aberration is monitored and evaluated by measuring the image distortion of the DT test pair A.

[0006] During the fabrication of DT capacitor devices, the image of the DT test pair A is affected by so-called three-foil (3-foil) aberration. However, in the meantime, the image of the DT test pair A is also affected by COMA aberration when using the same optical system. COMA is an aberration, which results in a point object being turned into a pear-shape or comet shape at the focal plane, most commonly off-axis. It is caused by unequal magnification in different zones of a lens for obliquely incident rays from an off-axis object. It is also known in the art that COMA aberration typically results in asymmetric photoresist image patterns in a photoresist layer for the originally sym-

metric patterns on the photo mask. The above-described prior art test key layout 10 for monitoring lens aberrations is not capable of abstracting the 3-foil aberration effect. Consequently, there is a need in this industry to provide an improved test key layout for precisely and exclusively monitoring single lens aberration effect, but not combined lens aberration effect, during the fabrication of DT capacitor devices.

SUMMARY OF INVENTION

[0007] It is therefore the primary object of the present invention to provide a test key layout for precisely monitoring a 3-foil lens aberration during the fabrication of DT capacitor devices by eliminating the COMA aberration.

[0008] According to the claimed invention, an H-shaped test key layout is provided. A first test pattern is substantially disposed at a center position of a test key area. The first test pattern consists of a pair of rectangular shaped symmetric patterns having a length L and a width L. The test key area comprises a reference X-Y coordinate. A second test pattern (corner pattern) is arranged in close proximity to the first test pattern in 45-degree directions with respect to the first test pattern. A third test pattern is disposed next to the first test pattern along an X-axis of the reference

X-Y coordinate. The first test pattern, second test pattern, and third test pattern are arranged like capital "H" within the test key area.

[0009] It is an unexpected benefit of the present invention that by adding the third test pattern next to first test pattern along the reference X-axis, the COMA aberration effect can be eliminated, thereby exclusively monitoring the 3-foil aberration effect during the fabrication of DT capacitor devices.

[0010] Other objects, advantages and novel features of the invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0011] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0012] Fig.1 is an enlarged plan view of a conventional test key layout for monitoring lens aberrations that occur during the fabrication of DT capacitor devices;

[0013] Fig.2 is a schematic plan view of a test key layout for monitoring lens aberrations during the fabrication of DT capacitor devices according to the first preferred embodiment of this invention; and

[0014] Fig.3 is a schematic plan view of a test key layout for monitoring lens aberrations during the fabrication of DT capacitor devices according to the second preferred embodiment of this invention.

DETAILED DESCRIPTION

[0015] The present invention pertains to a test key layout or pattern, which may be made on a photomask or be transferred through the photomask containing the test key layout to a photoresist layer coated on a wafer. The present invention is particularly suited for monitoring the 3-foil aberration during the fabrication of DT capacitor devices with an optical lithographic system utilizing a high numerical aperture (NA) such as NA>0.7 and an off-axis illumination such as QUASAR 90, but not limited thereto.

[0016] Please refer to Fig.2. Fig.2 is a schematic plan view of a test key layout 100 for monitoring lens aberrations during the fabrication of DT capacitor devices according to the first preferred embodiment of this invention, wherein like numerals designate the same or similar regions or ele-

ments. As shown in Fig.2, the test key layout 100 comprises a plurality of DT test pairs including pair A, pair B, pair C and pair D arranged in test key area 20. Generally, the test key area 20 is defined on a scribe line of a wafer or on peripheral region of a die (not shown). Each of the pairs A, B, C and D comprises a left side DT pattern 12 and a right side DT pattern 14. Both of the left side DT pattern 12 and right side DT pattern 14 are rectangular shaped and, as specifically indicated, have a length L and width W. According to the preferred embodiment, the dimension (length L and width W) of the left side DT pattern 12 and right side DT pattern 14 and the dimension of the DT capacitors made in the memory array are substantially the same. By way of example, for a 0.11-micron process, the length L of the left side DT pattern 12 and right side DT pattern 14 is 220nm, and the width W of the left side DT pattern 12 and right side DT pattern 14 is 110nm. On a photomask, the left side DT pattern 12 and right side DT pattern 14 are opaque regions. Light irradiating the test key area 20 passes through the photomask substrate except the opaque left side DT pattern 12 and right side DT pattern 14.

[0017] According to the present invention, the pair A is substan-

tially disposed at a center position of the test key area 20, the pair B is arranged in 45 degree direction with respect to the pair A in the test key area 20, while the pair C is substantially disposed in 45 degree direction with respect to the pair B. The pair A and pair C are aligned with a reference Y-axis. As seen in Fig.2, the pair C is disposed a distance (spacing) S_1 from the pair A along the ±Y-axis (supposing that the pair A is located on the coordinate origin of the reference X-Y axis coordinate system). In accordance with the preferred embodiment of this invention, the length L of the left side DT pattern 12 and right side DT pattern 14 is three times the spacing S_1 between the pair A and pair C (i.e., S_1=3L). In the indicated circle region 30, i.e., the area substantially surrounded by the pair A and pair B, DT test pair D is disposed therein. The pair A and pair D are aligned with a reference X-axis. As seen in Fig.2, the pair D is disposed a distance from the pair A along the ±X-axis.

[0018] The pair D is disposed a distance S_2 from the pair B. In accordance with the preferred embodiment of this invention, the length L of the left side DT pattern 12 and right side DT pattern 14 is substantially equal to the spacing S_2 between the pair B and pair D (i.e., S_2=L). As specifically in-

dicated, the spacing between the left side DT pattern 12 of the pair A and the right side DT pattern 14 of the pair D is denoted as "S_3". In accordance with the preferred embodiment of this invention, the spacing S_3 is substantially equal to the width W of the left side DT pattern 12 and right side DT pattern 14 (i.e., S_3=W). The arrangement of the pairs A, B, and D is somewhat like a capital "H" within the test key area 20 (H-shaped layout).

[0019] It is an unexpected benefit of the present invention that by adding the DT test pair D inside the circle regions 30 next to the pair A, the COMA aberration effect can be eliminated, thereby enabling exclusively monitoring of the 3-foil aberration effect during the fabrication of DT capacitor devices.

[0020] Please refer to Fig.3. Fig.3 is a schematic plan view of an H-shaped test key layout 102 for monitoring 3-foil lens aberration during the fabrication of DT capacitor devices according to the second preferred embodiment of this invention, wherein like numerals designate the same or similar regions or elements. Comparing to the first preferred embodiment, the second preferred embodiment as depicted in Fig.3 is a further simplified version. As shown in Fig.3, the H-shaped test key layout 102 comprises a

central DT test pair A, and single DT test pattern B" and single DT test pattern D" arranged in the test key area 20. Generally, the test key area 20 is defined on a scribe line of a wafer or on peripheral region of a die (not shown).

[0021] The central DT test pair A comprises a left side DT pattern 12 and a right side DT pattern 14. The left side DT pattern 12 and right side DT pattern 14, the single DT test pattern (corner pattern) B' and single DT test pattern (COMA eliminating pattern) D' are all rectangular shaped and, as specifically indicated, have a length L and width W. According to the preferred embodiment, the dimension (length L and width W) of the left side DT pattern 12 and right side DT pattern 14 and the dimension of the DT capacitors made in the memory array are substantially the same. By way of example, for a 0.11-micron process, the length L is about 220nm, and the width W is about 110nm. On a photomask (not shown), the left side DT pattern 12, right side DT pattern 14, the single DT test pattern B' and single DT test pattern D' are opaque regions. Light irradiating the test key area 20 passes through the transparent photomask substrate except the opaque regions.

[0022] According to the second preferred embodiment of the

present invention, the DT test pair A is substantially disposed at a center position of the test key area 20, the single DT test pattern B' is arranged in 45 degree direction with respect to the DT test pair A in the test key area 20. In the circle region 30, i.e., the area substantially defined by the DT test pair A and corner pattern B', single DT test pattern D' is disposed therein. The DT test pair A and single DT test pattern D' are aligned with a reference X-axis. As seen in Fig.3, the single DT test pattern D' is disposed a distance S_3 from the pair A along the ±X-axis. In accordance with the second preferred embodiment of this invention, the length L is substantially equal to the spacing S_2 (i.e., S_2=L). The spacing S_3 is substantially equal to the width W (i.e., S_3=W). The arrangement of the pair A, single DT test pattern B', and single DT test pattern D' is somewhat like a capital "H" within the test key area 20 (H-shaped layout).

[0023] Those skilled in the art will readily observe that numerous modification and alterations of the present invention may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.